FADE CONTROLLER FOR PROVIDING PROGRAMMABLE FADE RATES FOR ON-SCREEN DISPLAY (OSD) WINDOW

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to circuitry for controlling the display of an on-screen display (OSD) window within a video display, and in particular, to fade control circuitry for providing fade in and fade out control over an OSD window.

2. Description of the Related Art

[0002] Referring to Figure 1, as video display devices have increased in complexity and sophistication, particularly computer monitors, it is increasingly common for the display 10 in which a video image 12 is displayed to also include an OSD region, or window, 20 in which OSD information is displayed, such as one or more lines of OSD characters. One feature which has become increasingly popular is fading of the OSD window 20, whereby the vertical 20v and 20h dimensions of the OSD window 20 are selectively increased (fade in) or decreased (fade out) when opening or closing, respectively, the OSD window 20. This is typically done by initiating the opening and terminating the closing at the top left corner 20c of the OSD window 20. Between its fully closed and fully opened states, the OSD window will have a number of intermediate sizes as indicated by the dashed lines 20vi, 20hi representing the intermediate vertical and horizontal dimensions of such intermediate windows.

[0003] Opening or closing of the OSD window 20 is normally timed to be less than one second, e.g., approximately 0.5 second. The time intervals for the opening or closing of the window 20 in the horizontal and vertical directions can be fixed, or variable dependent upon the size of the window 20. While fixing such time interval would make the implementation of the control circuitry for doing this a simpler task, the size and shapes of OSD windows 20 are often variable. Accordingly, using fixed time intervals would cause the opening and closing times for a small OSD window to be faster than for a larger window. Hence, for a small OSD window, the resulting fade in and fade out effects would appear minimal.

SUMMARY OF THE INVENTION

[0004] In accordance with the presently claimed invention, a fade controller provides programmable fade rates for an on-screen display (OSD) window within a video display. Simple digital circuitry is used to control the size and dimensions of the OSD window and the rates at which it opens vertically and horizontally for fade in or closes vertically and horizontally for fade out, or both.

[0005] In accordance with one embodiment of the presently claimed invention, a fade controller for providing programmable fade rates for an OSD window within a video display includes accumulation circuitry, counting circuitry and encoding circuitry. The accumulation circuitry responds to reception of a plurality of accumulation control signals and respective programmable vertical and horizontal fade interval data signals corresponding to respective programmable vertical and horizontal OSD fade intervals by providing respective pluralities

of cumulative vertical and horizontal fade interval data signals corresponding to respective pluralities of cumulative vertical and horizontal OSD fade intervals. The counting circuitry, coupled to the accumulation circuitry, responds to reception of a plurality of timing control signals and the pluralities of cumulative vertical and horizontal fade interval data signals by providing vertical and horizontal count signals corresponding to respective completions of the cumulative vertical and horizontal OSD fade intervals. The encoding circuitry, coupled to the counting circuitry, responds to reception of a plurality of OSD window control signals and the vertical and horizontal count signals by providing an OSD fade control signal corresponding to occurrence of the OSD window within the video display.

[0006] In accordance with another embodiment of the presently claimed invention, a fade controller for providing programmable fade rates for an OSD window within a video display includes accumulator means, counter means and encoder means. The accumulator means is for receiving a plurality of accumulation control signals and respective programmable vertical and horizontal fade interval data signals corresponding to respective programmable vertical and horizontal OSD fade intervals and in response thereto generating respective pluralities of cumulative vertical and horizontal fade interval data signals corresponding to respective pluralities of cumulative vertical and horizontal OSD fade intervals. The counter means is for receiving a plurality of timing control signals and the pluralities of cumulative vertical and horizontal fade interval data signals and in response thereto generating vertical and horizontal count signals corresponding to respective completions of the cumulative vertical and horizontal OSD fade intervals. The encoder means is for receiving a plurality of OSD window control signals and the vertical and

horizontal count signals and in response thereto generating an OSD fade control signal corresponding to occurrence of the OSD window within the video display.

[0007] In accordance with still another embodiment of the presently claimed invention, a method of fade control for applying programmable fade rates to an on-screen display (OSD) window within a video display includes:

vertically fading the OSD window using a programmable vertical OSD interval value corresponding to a vertical dimension of the OSD window; and

horizontally fading the OSD window using a programmable horizontal OSD interval value corresponding to a horizontal dimension of the OSD window;

with each of the fadings performed by

providing the programmable OSD interval value;

storing the programmable OSD interval value;

enabling the OSD window;

counting during a time interval corresponding to the stored OSD interval value;

disabling the OSD window following termination of the time interval count;

combining the programmable and stored OSD interval values to provide a cumulative OSD interval value;

substituting the cumulative OSD interval value for the stored OSD interval value;

repeating the enabling, counting, disabling, combining and substituting until a predetermined cumulative OSD interval value has been reached.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a diagram illustrating the display of an OSD window within a video display.

Figure 2 is a functional block diagram of that portion of a video display system employing a fade controller in accordance with the presently claimed invention.

Figure 3 is a functional block diagram of a fade controller in accordance with one embodiment of the presently claimed invention.

Figure 4 is a state diagram depicting the states and transitions between states for the horizontal control sequencer in the circuit of Figure 3.

Figure 5 is a state diagram depicting the states and transitions between states for the vertical control sequencer in the circuit of Figure 3.

DETAILED DESCRIPTION OF THE INVENTION

[0008] The following detailed description is of example embodiments of the presently claimed invention with references to the accompanying drawings. Such description is intended to be illustrative and not limiting with respect to the scope of the present invention. Such embodiments are described in sufficient detail to enable one of ordinary skill in the art to practice the subject invention, and it will be understood that other embodiments may be practiced with some variations without departing from the spirit or scope of the subject invention.

[0009] Throughout the present disclosure, absent a clear indication to the contrary from the context, it will be understood that individual circuit elements as described may be

singular or plural in number. For example, the terms "circuit" and "circuitry" may include either a single component or a plurality of components, which are either active and/or passive and are connected or otherwise coupled together (e.g., as one or more integrated circuit chips) to provide the described function. Additionally, the term "signal" may refer to one or more currents, one or more voltages, or a data signal. Within the drawings, like or related elements will have like or related alpha, numeric or alphanumeric designators. Further, while the present invention has been discussed in the context of implementations using discrete electronic circuitry (preferably in the form of one or more integrated circuit chips), the functions of any part of such circuitry may alternatively be implemented using one or more appropriately programmed processors, depending upon the signal frequencies or data rates to be processed.

[00010] When using a fixed interval for the fading in and fading out of the OSD window, such interval can be determined by establishing the total fade in or fade out time interval and the typical size of the OSD window. For example, a common size for a single OSD character is twelve pixels in width and eighteen lines in height. Accordingly, by knowing how many characters are to be available for each horizontal line and how many lines of characters are to be available, the size of the OSD window can be readily determined. By fixing the number of pixels and lines to be opened or closed during each vertical field or scan, appropriate circuitry can be readily implemented. However, as noted above, using a fixed interval is may be undesirable when variable OSD window sizes are possible.

[00011] To determine the appropriate horizontal fade interval, the horizontal dimension in pixels would be divided by the product of the average fade (in and out) time and the average vertical scan rate. Similarly, for the appropriate vertical fade interval, the vertical

dimension in lines would be divided by the product of the average fade (in and out) time and the average vertical scan rate.

[00012] For example, for a fade (in/out) time of one second and a vertical scan rate of 60 Hertz, the horizontal and vertical intervals can be computed as follows. For a horizontal dimension of 600 pixels, the horizontal interval would equal 600/(1.0*60) = 10 pixels, while for a vertical dimension of 480 lines, the vertical interval would equal 480/(1.0*60) = 8 lines. Accordingly, four bits for the vertical and horizontal interval number would be sufficient. For even more control on fade in/out speed, the register used for the interval data can be increased, e.g., an eight-bit register.

[00013] Referring to Figure 2, using the more desirable variable fade interval requires determining the size of the OSD window. For implementation in hardware, an auto-size functional stage 32 determines the size of the OSD window by monitoring pertinent timing signals within the video display system; horizontal flyback 31h; vertical flyback 31v; pixel clock 31p; OSD enable 31o; fade (in/out) enable 31f; and a master OSD function enable 31e.

[00014] The resulting horizontal 33h and vertical 33v size data are then divided in a divider stage 34 by the desired interval value and average vertical scan rate (as noted above) to produce the appropriate horizontal 35h and vertical 35v interval data. As discussed in more detail below, the fade in/out stage 36 then uses these horizontal 35h and vertical 35v interval data to produce the appropriate OSD fade control signal 37.

[00015] Such an auto-sizing stage 32 can be implemented in any of a number of well known conventional ways. Alternatively, the auto-sizing functional stage 32 can be implemented in firmware by using some form of computational stage (e.g., microprocessor or

microcontroller) to perform the above-discussed computations needed to produce the horizontal 35h and vertical 35v interval data.

[00016] An additional advantage of having separately programmable interval numbers is the possibility for different fade in and fade out effects, such as horizontal fade only, vertical fade only, or both. For example, for vertical fade only, the horizontal register would be loaded with an interval data value of zero and the remaining hardware would detect this condition and immediately open the OSD window horizontally in full. Similarly, for horizontal fade only, the vertical interval data would be programmed with a zero value, and the OSD window would immediately open vertically in full.

[00017] Referring to Figure 3, a fade controller 36 in accordance with the presently claimed invention includes fade control circuitry 40 and horizontal 60h and vertical 60v control sequencing circuitry. In turn, the fade control circuitry 40 includes horizontal fade control circuitry 40h and vertical fade control 40v. As discussed in more detail below, the horizontal control sequencer 60h and vertical control sequencer 60v provide various control and timing signals 61h, 61v for the horizontal 40h and vertical 40v fade control circuitry, respectively.

[00018] Each of the horizontal 40h and vertical 40v fade control circuits includes a digital adder 42, a signal router (e.g., switch or multiplexor) 44h, a multi-bit register 46, a counter 48 and a latch 50, all interconnected substantially as shown. In each circuit 40h, 40v, the incoming programmable interval data 35 (M bits for the horizontal interval data 35h and P bits for the vertical interval data 35v) are received by the adder 42 and router 44. The

routed, or selected, data 45 is stored in the register 46. The stored data 47 is fed back to the other input of the adder 42 and is also loaded into the counter 48.

[00019] Control signal 61a from the sequencer 60 determines whether the adder 42 is used to find the sum of or take the difference between the programmable interval data 35 and the previously stored data 47. These data 35, 47 are added for fade in, and are subtracted (e.g., programmable data 35 subtracted from stored cumulative data 47) for fade out.

[00020] Control signal 61b selects between the programmable interval data 35 and the combined (added or subtracted) data 43 and provides such selected data 45 to the register 46 for storage as cumulative data 47. Control signal 61b is initially inactive (e.g., de-asserted) to cause the incoming interval data 35 to be loaded into the register 46. Subsequently, it becomes active (e.g., asserted) so as to allow the data 47 stored in the register 46 to become cumulative based upon the operation of the adder 42.

[00021] A clocking, or loading, signal 61c for the register 46 is active in relation to the vertical flyback signal 31v, and becomes inactive once the maximum OSD dimension (horizontal or vertical) has been reached.

[00022] Control signal 61d loads the stored cumulative data 47 into the counter 48. Control signal 61dh for the horizontal circuitry 40h is related to the horizontal feedback signal 31h, while control signal 61dv for the vertical circuitry 40v is related to the vertical flyback signal 31v. Control signal 61e clocks the counter 48 which, upon completing its count, activates its terminal count output signal 49. Control signal 61eh for the horizontal circuitry 40h is related to the pixel clock signal 31p, while control signal 61ev for the vertical circuitry 40v is related to the horizontal flyback signal 31h.

[00023] In a preferred embodiment, the counter circuitry 48 is a down counter and the terminal count signal 49 is active, e.g., asserted, upon the attainment of a zero count. However, it will be appreciated that, if the complement of the stored cumulative data 47 is available for use by the counter 48, such counter 48 can also be an up counter with the terminal count signal 49 becoming active following attainment of a maximum count value.

[00024] The terminal count signal 49 is latched by the latch circuitry 50 in accordance with its clock signal 61f, where both clock signals 61fh, 61fv are frequency-divided versions (e.g., one-fourth) of the pixel clock signal 31p.

[00025] The resulting latched signals 51h, 51v are logically ANDed with each other and control signal 61gh. When asserted, this control signal 61gh indicates that the OSD window is to be faded (in/out), as opposed to being fixed. The resulting ANDed signal 53 is logically ORed with the inverse of control signal 61gh. Accordingly, during assertion of this control signal 61gh, the enabled combination of the two latched signals 51h, 51v effectively passes through the OR gate 54 to become a fade enablement signal 55 which is itself enabled by the OSD enablement signal 31o in an output AND gate 56, thereby producing the final OSD fade enablement signal 37.

[00026] Hence, in conformance with the foregoing discussion, each of the horizontal 40h and vertical 40v fade control circuits operates as follows. The incoming programmable interval data 35 is routed by the router 44 and initially stored in the register 46. This stored data 47 is used by the counter 48 to establish the initial fade interval. For fade in, this initial fade interval is the minimum interval, while for fade out, this initial interval is the maximum interval. During the next vertical scan interval, the stored interval data 47 is fed back and

combined with a programmable interval data 35 (summed for fade in and subtracted for fade out), with the resulting combined interval data 43 being routed by the router 44 to the register 46 for storage as cumulative interval data 47. This newly computed cumulative interval data 47 is then used by the counter 48 to establish the next fade interval. This process continues until the maximum (fade in) or minimum (fade out) OSD dimension is reached.

[00027] The horizontal 60h and vertical 60v control sequencers can be implemented as state machines in accordance with well known techniques. Referring to Figure 4, a state machine for implementing the horizontal control sequencer 60h includes a plurality of machine states 100 as follows. Operation begins with an idle state 102. Transition 103a occurs when fade in is enabled and the programmable horizontal interval data 35h is non-zero. If these conditions are not true, transition 103b occurs, thereby maintaining the idle state 102.

[00028] During state 104, fade in is enabled and the occurrence of an active OSD window is awaited. Transition 105a occurs when an active OSD window is to be faded, e.g., as when control signal 61gh (Figure 3) is active. Meanwhile, until the OSD window is active, transition 105b occurs during which the stored interval data 47h remains equal to the original programmable data 35h.

[00029] During state 106, fade in remains enabled and an active OSD enablement signal is awaited. Upon enablement of a faded OSD window, transition 107a occurs. Until then, transition 107b occurs and the counter 48h is loaded with the stored interval data 47h. If no faded OSD window is to be displayed, transition 107c occurs, thereby placing the system in state 112.

[00030] During state 112, vertical flyback is awaited. Upon occurrence of vertical flyback, transition 113a occurs, horizontal interval data is accumulated and the system is returned to state 104. Meanwhile, until vertical flyback does occur, transition 113b causes the system to remain in state 112.

[00031] In state 108, the counter 48h performs its count function based upon the loaded interval data 47h. Upon the occurrence of terminal count, transition 109a occurs. Meanwhile, until terminal count is achieved, transition 109b occurs with the counter continuing its count sequence.

[00032] During state 110, the OSD window is not displayed. Transition 111a occurs when the OSD fade enablement signal becomes inactive, thereby causing the system to return to state 106 and the counter 48h to be reloaded with the accumulated interval data 47h. Until then, transition 111b occurs and the system remains in state 110.

[00033] During state 108, if either of the OSD enablement or faded OSD enablement signals become inactive, transition 109c occurs, the difference between the present accumulated interval data 47h and the programmable interval data 35h is substituted as the data for the counter 48h and the system enters state 114.

[00034] In state 114, the system awaits enablement of the fade out operation. Upon enablement of the fade out, transition 115a occurs. Meanwhile, transition 115b occurs, keeping the system in state 114. However, if vertical fade out is completed, transition 115c occurs and the system returns to the idle state 102.

[00035] During state 116, enablement of the OSD window is awaited. Upon such concurrence, transition 117a occurs. Meanwhile, transition 117b occurs, maintaining the system in state 116. However, if the OSD window is no longer vertically active, transition 117c occurs.

[00036] In state 118, the counter performs its count sequence. Upon attainment of terminal count, transition 119a occurs. Meanwhile, transition 119b occurs and the counter continues its count sequence.

[00037] In state 120, fade out has occurred and so long as the OSD fade function is enabled transition 121b maintains the system in state 120. Following disablement of the OSD fade function, transition 121a occurs, returning the system to state 116.

[00038] During state 122, fade out is enabled and vertical flyback is awaited. Transition 123a occurs if the difference between the accumulated interval data 47h and the programmable interval data 35h becomes zero or negative, or if vertical fade out has been completed, following which the system enters state 124. Otherwise, if vertical flyback has not yet occurred, transition 123b maintains the system in state 122. Upon occurrence of vertical flyback, transition 123c occurs, the difference between the accumulated interval data 47h and programmable interval data 35h is computed and stored, and the system returns to state 114. If fade out is no longer enabled, transition 123d occurs and the system returns to the idle state 102.

[00039] In state 124, fade out is completed. If fade out is no longer enabled, transition 125a returns the system to the idle state 102. Meanwhile, so long as fade remains enabled, transition 125b maintains the system in state 124.

[00040] Referring to Figure 5, a state machine for implementing the vertical sequencer 60v includes a plurality of machine states 200 as follows. The system begins in its idle state 202. Upon concurrence of enablement of the fade in function and non-zero programmable interval data 35v, transition 203a occurs. Until such concurrence, transition 203b maintains the system in its idle state 202.

[00041] In state 204, fade in is enabled and OSD enablement is awaited. Following enablement of the OSD window, transition 205a occurs. Until such enablement, transition 205b maintains the system in state 204 and the programmable vertical interval data 35v is stored in the register 46v. If the fade in function becomes disabled, transition 205c causes the system to enter state 210. During this transition 205a, the counter is loaded with the stored vertical interval data.

[00042] In state 206, the count sequence is initiated. Upon attainment of terminal count, transition 207a occurs. Until terminal count is attained, transition 207b occurs and the count sequence continues. In the event that the fade in function is disabled and the OSD window is no longer active, transition 207c occurs, causing the system to enter state 210.

[00043] In state 208, fade in is complete and vertical flyback is awaited. Following vertical flyback, transition 209a occurs, the accumulated 47v and programmable vertical interval 35v data are added, and the system returns to state 204. Meanwhile, pending vertical flyback, transition 209b maintains the system in state 208. In the event that the fade in function becomes disabled, transition 209c causes the system to enter state 210.

[00044] In state 210, enablement of the fade function is awaited. Following enablement, transition 211a occurs. Until such enablement, transition 211b maintains the

system in state 210 and the difference between the accumulated 47v and programmable vertical interval 35v data is computed and stored.

[00045] In state 212, fade out is enabled and enablement of the OSD window is awaited. Once the OSD window becomes active, transition 213a occurs. During this transition 213a, the counter 48v is loaded with the stored vertical interval data 47v. Until then, transition 213b maintains the system in state 212. In the event that the horizontal state is completed and the difference between the accumulated and programmable vertical interval data is zero or negative, transition 213c occurs and the system enters state 218.

[00046] In state 214, fade out is initiated and the counter begins its count sequence. Upon attainment of terminal count, transition 215a occurs. Until terminal count is attained, transition 215b occurs and the count sequence continues.

[00047] In state 216, fade out is completed and vertical flyback is awaited. Following vertical flyback, transition 217a occurs, the difference between the previously stored 47v and programmable vertical interval 35v data is computed and stored as present accumulated data 47v, and the system returns to state 212.

[00048] In state 218, fade out is completed. Following disablement of the fade function, transition 219a returns the system to its idle state 202. Until then, transition 219b maintains the system in state 218.

[00049] Various other modifications and alternations in the structure and method of operation of this invention will be apparent to those skilled in the art without departing from the scope and the spirit of the invention. Although the invention has been described in

connection with specific preferred embodiments, it should be understood that the invention as claimed should not be unduly limited to such specific embodiments. It is intended that the following claims define the scope of the present invention and that structures and methods within the scope of these claims and their equivalents be covered thereby.